DESIGN AND ANALYSIS OF NOVEL CHARGE PUMP ARCHITECTURE FOR PHASE LOCKED LOOP

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

in

VLSI Design and Embedded Systems

By

SWANAND VISHNU SOLANKE

ROLL NO. 207EC208

Department of Electronics and Communication Engineering

National Institute Of Technology

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Under the Guidance of

Prof. D. P. ACHARYA

Department of Electronics and Communication Engineering

National Institute Of Technology

Rourkela

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Rourkela

CERTIFICATE

This is to certify that the thesis entitled, **"Design and Analysis of Novel Charge Pump Architecture For Phase Locked Loop"** submitted by **Swanand Vishnu Solanke** in partial fulfilment of the requirements for the award of Master of Technology Degree in Electronics & Communication Engineering with specialization in **"***VLSI Design and Embedded System***"** at the National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

Date:

Prof. D. P. Acharya
Dept. of Electronics & Communication Engg.
National Institute of Technology
Rourkela-769008

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SWANAND VISHNU SOLANKE

ROLL No: 207EC208

Contents

Abstract

Modern wireless communication systems employ Phase Locked Loop (PLL) mostly for synchronization, clock synthesis, skew and jitter reduction. The performance of PLL affects significantly the signal recovery and system functionality in these systems. Charge pump being one of the important components, decides the functional parameters of PLL. This thesis simulates and analyses some of the major reported charge pump architectures. The present work also proposes an efficient architecture of CMOS charge pump and analyses the design considerations for the proposed circuit. The novel charge pump is designed in Cadence Virtuoso environment and implemented using GPDK090 library of 0.1µm technology and a supply voltage of 1.8V. The performance parameters are compared with other standard and latest charge pump based architectures of PLL. The PLL implemented using proposed charge pump is found to exhibit very low acquisition time of 850ns and consume substantially low power of 0.6041mW.

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Chapter 1

Introduction

Motivation

Phase locked loop, popularly known as PLL [1] is one of the important constituent of modern electronic systems. Having wide range of applications over a broad frequency spectrum PLL has become one of the most essential element [2] in microprocessor boards of complex systems, wired and wireless communication systems and many other systems.

Earliest research towards what became known as the phase-locked loop goes back to 1932 [3], when British researchers developed an alternative to Edwin Armstrong's super heterodyne receiver, the Homodyne or direct-conversion receiver. In the homodyne or synchrodyne system, a local oscillator was tuned to the desired input frequency and multiplied with the input signal. The resulting output signal included the original audio modulation information. The intent was to develop an alternative receiver circuit that required fewer tuned circuits than the super heterodyne receiver. Since the local oscillator would rapidly drift in frequency, an automatic correction signal was applied to the oscillator, maintaining it in the same phase and frequency as the desired signal. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal *Onde Electrique*.

In analog television receivers since at least the late 1930s, phase-locked-loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal. When Signetics introduced a line of monolithic integrated circuits that were complete phase-locked loop systems on a chip in 1969, applications for the technique multiplied. A few years later RCA introduced the "CD4046" CMOS Micropower Phase-Locked Loop, which became a popular integrated circuit.

Since its invention, the design of PLL has remained challenging because of requirement of fast, low power consuming and less noisy electronic equipments. “Charge Pump” is one essential part of PLL. Charge pump (CP) converts the phase or frequency

difference information of two input signal into a voltage which is used to tune a "Voltage Controlled Oscillator" toward reference input frequency. Other elements of PLL are "Phase Frequency Detector (PFD)", "Low Pass Filter (LPF)" and "Voltage Controlled Oscillator (VCO)". Implementation of LPF is very easy while PFD and VCO can be implemented in static CMOS logic. But being a current driven system, charge pump finds to be more challenging for implementation, since performance of CP directly affects the speed, power consumption and noise behaviour of PLL. Clock feed through, charge sharing, current mismatch are some of the challenges in design of CP. Charge pump is one of the most popular topics in research of solid state electronics, wireless communication etc. and so many different architectures are proposed which claim to be robust and more efficient. The challenges in design of efficient charge pump motivated me towards the research in this field. In this work a novel architecture of CP which is efficient in terms of power consumption, speed and noise is proposed.

Outline of the Thesis

It is important to understand the whole PLL system before going into the details of CP. Chapter 2 briefly describes the basics of PLL. A mathematical model of PLL is produced in section 2.1 which makes understanding of PLL easier. Since PLL is feedback system, a control theory approach is used to form the mathematical model of PLL. Section 2.2 gives the basic terminology of PLL while in consecutive sections types of PLL, non ideal effects related to PLL, its applications are discussed in brief.

Chapter 3 builds the concepts of charge pump. Section 3.2 and 3.3 gives the brief outline of concept of building a charge pump and necessity of PFD. Section 3.4 describes the mathematical theory related to the charge pump PLL. After discussing the basic charge pump architecture in 3.6, its non ideal effects are discussed in section 3.7. In section 3.8 comparison

between single ended and differential charge pump is given. Section 3.9 briefly discusses the different architectures of charge pump and their performance.

The proposed charge pump architecture is described in Chapter 4. An introduction to self biased high swing cascode current mirror is given in section 4.1. Section 4.2 briefly discusses the design and simulation of proposed charge pump. Chapter 5 provides the conclusions that can be inferred out of this work.

Chapter 2

An overview of PLL

2.1 Theory of PLL

PLL is simple feedback system [4] that compares the output phase with the input phase and produces the output frequency which is proportional to the input phase difference. Since its invention in1932, the basic phase locked loop has remained nearly the same but its implementation in different technologies and for different applications continues to challenge designers. This topic deals with basics of PLL.

Fig. 2.1 shows the basic block diagram of PLL.

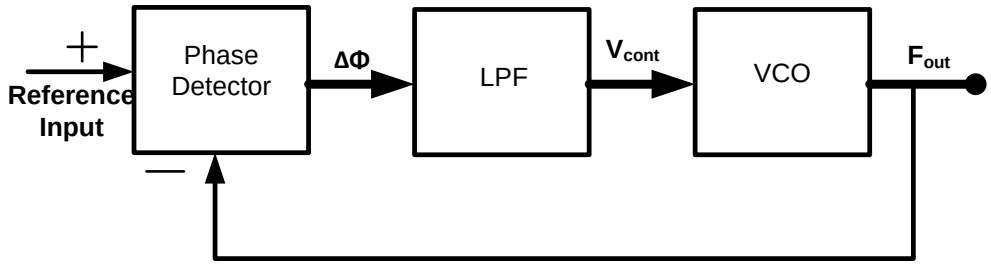

Fig. 2.1 Basic PLL Block Diagram

A phase detector is a circuit whose average output voltage is proportional to the phase difference $\Delta\phi$, between two inputs. In the ideal case relation between average output voltage and input phase difference is linear, crossing the origin for $\Delta\phi=0$ as shown in figure 2.2.

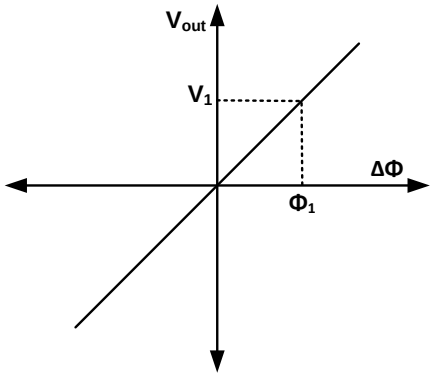

Fig. 2.2 Phase detector characteristics

Called the gain of PD is the slope of line, K_{PD}, which is expressed in V/rad.

The output of PD is then passed through a low pass filter, so as to remove the high frequency content in PD output voltage. This is required because; the control voltage of oscillator must remain quit in steady state. Filter also provides a memory for the loop in case lock is momentarily lost due to large interference transient.

This filtered control voltage is then applied to the input of Voltage Controlled Oscillator. Control voltage forces the VCO to change the frequency in the direction that reduces the difference between input frequency and output frequency. If two frequencies are sufficiently close, the PLL feedback mechanism forces the two PD input frequency frequencies to be equal and the VCO is locked with incoming frequency. This is called as locked state of PLL.

Fig. 2.3 depicts the basic operation of PLL.

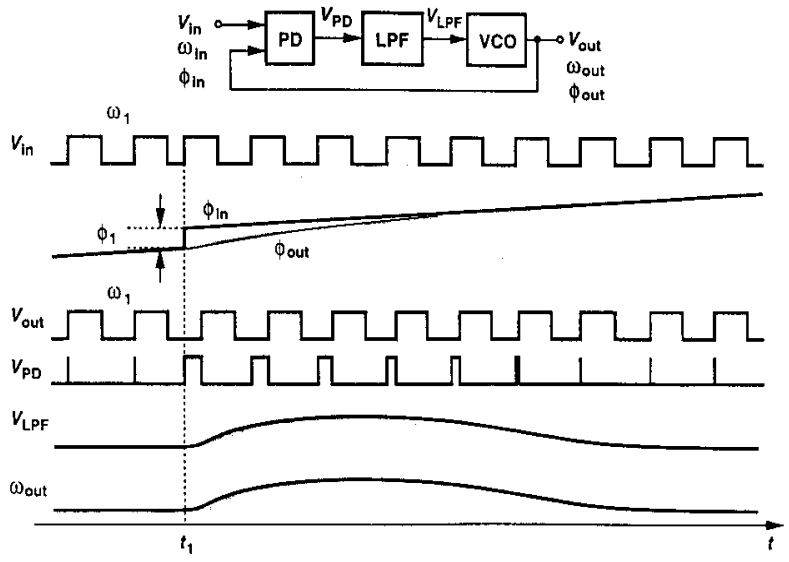

Fig. 2.3 Basic operation of PLL

Once the loop is in locked state, there will be small phase difference between the two PD input phase signals. This phase difference results in a dc voltage at the phase detector

output which is required to shift the VCO from its free running frequency to input frequency and keeps the loop in locked state.

2.1.1 Dynamics of simple PLL

A linear model of PLL can be constructed mathematically by considering figure 2.4, which shows the linear model of type I PLL. Low pass filter is assumed to be of first order for simplicity.

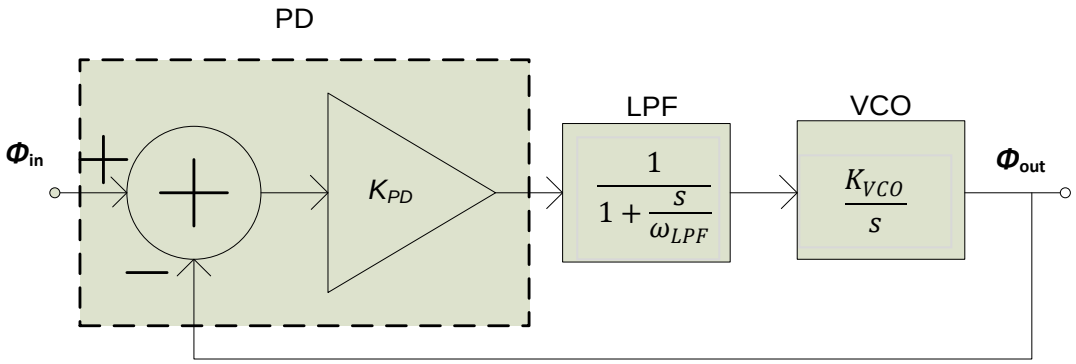

Fig. 2.4 Linear model of type I PLL

The PD output contains a dc component equal to $K_{PD}(\Phi_{out}-\Phi_{in})$ as well as high frequency components which are filtered by the LPF. PD is simply modeled as a subtractor whose output is amplified by K_{PD}. The overall PLL model consists of the phase subtractor, the LPF transfer function $1/(1+ s/\omega_{LPF})$, where ω_{LPF} is the 3 dB bandwidth and the VCO transfer function K_{VCO}/s. Here, Φ_{in} and Φ_{out} are the excess phases of input and output waveforms, respectively.

The open loop transfer function is given by

$$H(s)|_{open} = \frac{\Phi_{out}}{\Phi_{in}}(s)|_{open}$$

$$= K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s} \qquad (2.1)$$

From (2.1) closed loop transfer function can be obtained as:

$$H(s)|_{closed} = \frac{K_{PD}\,K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}\,K_{VCO}} \qquad (2.2)$$

Here $H(s)|_{closed}$ is simply denoted by $\Phi_{out}/\ \Phi_{in}$. Further, since the frequency and phase are related by a linear operator, the transfer function of (2.2) can be expressed as:

$$\frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}\,K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}\,K_{VCO}} \qquad (2.3)$$

This is second order transfer function of type I PLL. Using the control theory approach the "natural frequency" and "damping ratio" are given by:

$$\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}} \qquad (2.4)$$

$$\boldsymbol{\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}} \qquad (2.5)$$

The step response is given by:

$$\omega_{out}(t) = \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}t + \theta\right)\right]\Delta\omega u(t) \qquad (2.6)$$

Where ω_{out} denotes the change in output frequency and $\theta = \sin^{-1}\sqrt{1-\zeta^2}$. Thus, as per control theory approach, we can say that, the step response will contain a sinusoidal component with frequency $\omega_n\sqrt{1-\zeta^2}$ that will decay with time constant $(\zeta\omega_n)^{-1}$.

Referring to above discussion it can be concluded that:

1. Settling speed of PLL is of great concern in most applications. Equation (2.6) thus, shows that the exponential decay determines how fast the output approaches its final value, provided that $\zeta\omega_n$ is maximized.

   Using equation (2.4) and (2.5), yields,

   $$\zeta\omega_n = \frac{1}{2}\omega_{LPF} \qquad (2.7)$$

   This result shows the critical tradeoff between settling speed and ripple on the VCO control line. If we reduce the cutoff frequency of filter, greater high frequency components are suppressed but at the same time pull in time increases.

2. In addition to value of $\zeta\omega_n$, value of ζ is also important. If ζ is less than typically 0.5, step response exhibits high amplitude oscillations before settling. Hence in order to avoid this ringing, the value of damping ratio is normally kept 0.707 or even greater than or equal to 1.
3. Equation (2.5) shows that both phase error and ζ are inversely proportional to K_{PD} and K_{VCO}. Hence lowering the phase error makes the system less stable. Thus in summary the simple PLL (type I) has a drawback of trade off between the pull in time, the ripple on the control voltage, the phase error and the stability.

2.2 Terminology of PLL

1. Lock range:

The range of input signal frequencies over which the loop can maintain the lock is called as Lock Range or Tracking Range of PLL.

2. *Capture range:*

The range of input signal frequencies over which PLL can acquire a lock is called as Capture Range or Acquisition Range of PLL.

Capture range depends on the amount of the gain in a loop itself and the loop filter bandwidth. Reducing the loop filter bandwidth thus improves the rejection of the out of band signals, but at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

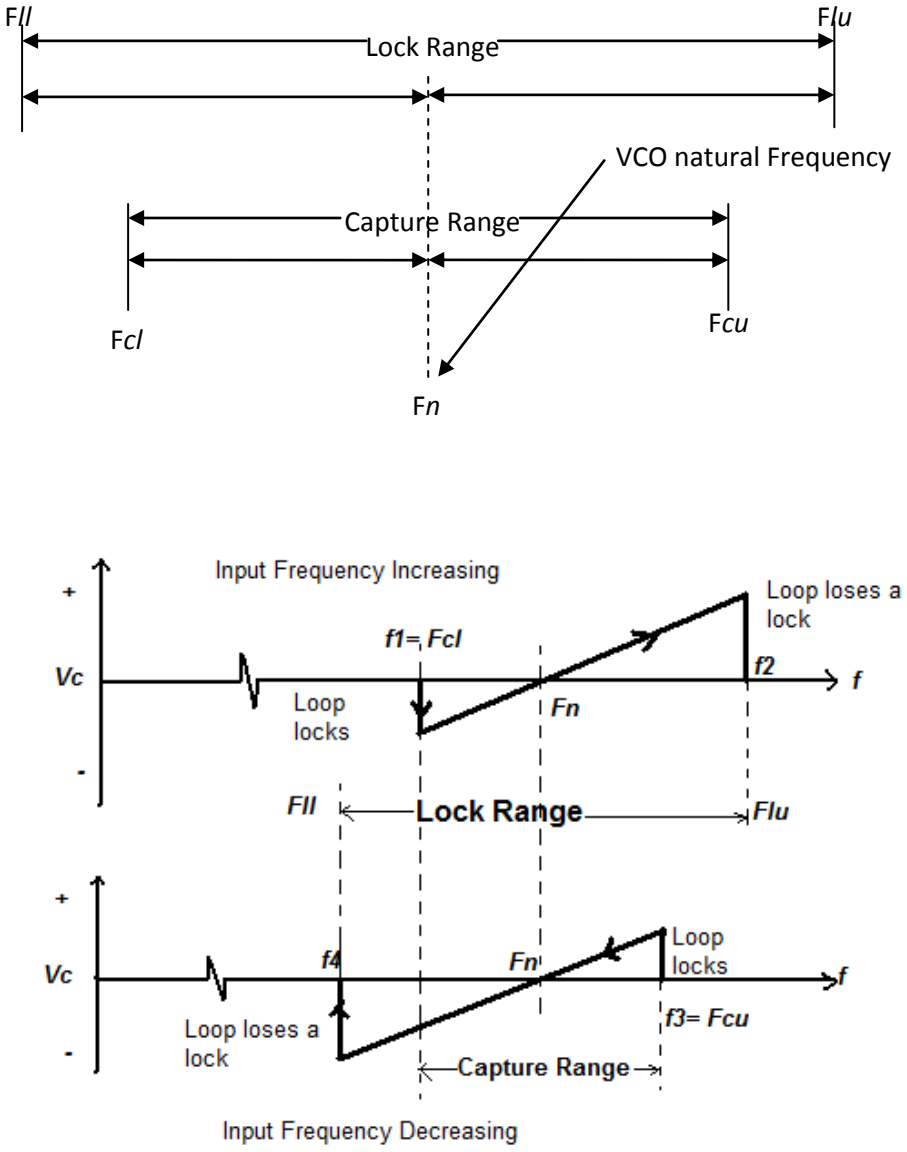

Fig.2.5 Illustration of Terminologies of PLL

3. Pull in time:

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

4. Band width of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

2.3 Types of PLL

Several types of PLL [5] architectures are available in market. The architectures broadly range according to the application. These different architectures of PLL can be considered as different types of PLL. Following types of PLL are classified according to their application.

1. Programmable PLL: This type of PLL can be programmed for wide range of signals.
2. Single and multi-phase PLL: These can control a single or many phases. They are used in digital clock networks.
3. Digital Phase Locked Loop: They are used digital input signals for application like Manchester coding.
4. PLL with lock detector: It uses a lock on one of the pins and is used in frequency modulation.
5. PLL frequency synthesizer: These are used to synthesize the frequency of different range and band.
6. PLL FM/AM demodulator: The FM/AM radio frequencies are modulated and demodulated using this type of PLL.
7. Single RF/ Multi RF PLL: It is used for controlling single or multiple radio frequencies.

8. Super PLL: It is used for frequency synthesizing of radios, networks of GSM, cordless phones, etc.

PLLs are also classified according to the type of loop filter used in architecture. The order of loop filter is the type of PLL. For example, if 1st order loop filter is used, then it is called as type I PLL. If 2nd order filter is used, it is called as type II PLL and so on.

If PLL uses simple 'Phase detector' in its architecture, it is called as simple PLL. But if PLL uses 'Phase Frequency Detector' accompanied with 'Charge Pump', it is called as "Charge Pump PLL".

2.4 Non Ideal Effects in PLL

So many imperfections always remain in practical PLL circuit. These lead to high ripple on the control voltage even when the loop is locked. These ripples modulate the VCO frequency, which results in non periodic waveform. This section considers these non ideal effects in PLL [4] [6] [7].

2.4.1 Jitter in PLL

A jitter is the short term-term variations of a signal with respect to its ideal position in time. This problem negatively impacts the data transmission quality. Deviation from the ideal position can occur on either leading edge or trailing edge of signal. Jitter may be induced and coupled onto a clock signal from several different sources and is not uniform over all frequencies. Excessive jitter can increase bit error rate (BER) of communication signal. In digital system Jitter leads to violation in time margins, causing circuits to behave improperly. Common sources of jitter include:

- Internal circuitry of PLL
- Random Thermal noise from crystal

- Other resonation devices
- Random mechanical noise from crystal vibration
- Signal transmitters
- Traces and cables
- Connectors
- Receivers

The response of PLL to jitter is very important in most applications. Figure 2.6 explains the jitter in PLL.

As shown in figure 2.6, a strictly periodic waveform, x1(t), contains zero crossings that are evenly spaced in time. Now consider nearly periodic signal x2(t), whose period experiences a small changes, deviating the zero crossing from their ideal points. Hence we can say that x2(t) suffers from jitter. If the instantaneous frequency of signal varies slowly from one period to next period, then it is called as "slow jitter", and if the variation is fast, it is called as fast jitter.

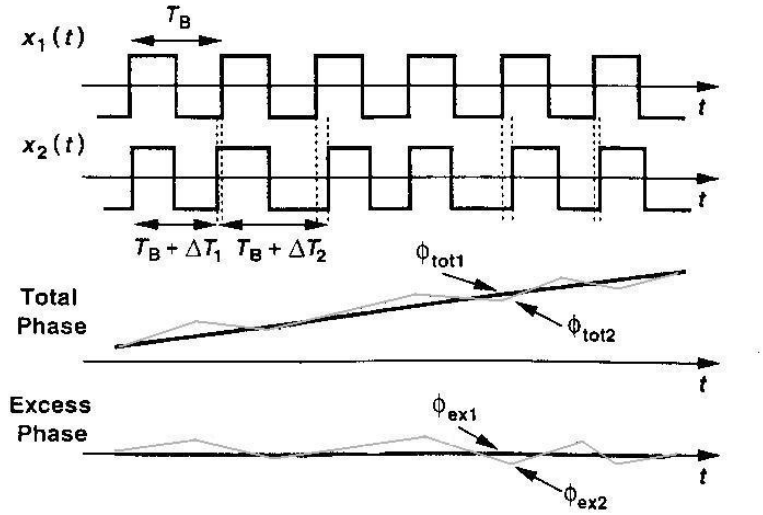

Fig. 2.6 Ideal and Jittery Waveforms

In PLL two types of phenomena are considered. a) The input exhibits jitter and b) The VCO produces jitter.

In first case, the transfer function derived for type I and type II PLLs have a low-pass characteristics, indicating that if $\Phi_{in}(t)$ varies rapidly, then $\Phi_{out}(t)$ does not fully track the variations. That means, slow jitter at the input propagates to the output unattenuated but fast jitter does not. That is, PLL low pass filters $\Phi_{in}(t)$.

Now suppose VCO suffers from jitter. If PLL is modelled for transfer function of Φ_{out}/Φ_{VCO} for type II, the transfer function depicts the high pass characteristics. That is, slow jitter components generated by VCO are suppressed but fast jitter components are not. If Φ_{VCO} changes slowly, then the comparison with perfectly periodic input waveform generates slowly varying error that propagates through LPF and adjusts the VCO frequency, thereby counteracting the change in Φ_{VCO}. On other hand if Φ_{VCO} varies rapidly, then error produced by the phase detector is heavily attenuated by the poles in loop, failing to correct the change.

2.4.2 Phase Noise

Phase noise is random variation of phase of the signal. It is the frequency domain representation of rapid, short term fluctuations in the phase of the wave, caused by time domain instabilities ("jitter"). Generally the phase noise and jitter are closely related. Or more specifically, radio engineer call it as phase noise, but digital system engineer call it as jitter of the clock. Phase noise is of very much concern in PLL, since it directly affects the entire performance of the system. Following are the common sources of phase noise in PLL.

i) **Oscillator noise**: There are two oscillators that contribute to the phase noise of the PLL. One is the reference oscillator and other is the VCO. Although both oscillators can be modelled similarly, their effects on the output noise are distinct just due to their position in the loop. Suppose a noise less VCO is added with AWGN with

DSPSD of $N_o/2$. Then the output power spectrum is given by $KVCO^2(N_o/2\omega^2)$. Though it is very simplified equation, it clearly gives the idea of output noise of PLL in the presence of VCO noise. The reference oscillator is also assumed to have sufficient behaviour with different constant of proportionality.

ii) **Frequency Divider noise**: The excess noise of a digital divider can be modelled as additive noise source at its output. In a PLL, this noise directly appears at the input of phase detector and experiences the same transfer function as the noise on the input terminal.

iii) **Phase detector noise**: Usually phase detectors are not major sources of noise in PLLs. As the work of PD is to detect the phase difference, any random variation in the phase of input signal makes the phase detector to produce wrong output, which is get transferred through filter and tunes the VCO wrongly.

2.4.3 Reference spur

Reference spurs are spurious emissions that occur from the carrier frequency at an offset equal to the channel spacing. These are usually caused by leakage and mismatch in charge pump of PLL. Though they occur outside the band of interest, they can enter the mixers and be translated back onto band of interest.

Reference spur mainly occurs in Charge Pump PLL. Though there is no phase difference between reference and feedback signal, in the locked state, the phase detector (or phase frequency detector) produces very narrow pulse width error voltage which drives the charge pump. Although these pulses have a very narrow width, the fact that they exist means that the dc voltage driving the VCO is modulated by a signal of frequency equal to input reference frequency. This produces **reference spurs** in the RF output occurring at offset frequencies that are integer multiples of input reference frequency. A spectrum analyzer can be used to detect reference spurs. Simply increase the span to greater than twice the reference frequency.

Let I_{cp} is charge pump current, I_{leak} is leakage current in CP then the phase offset is given by:

$$\Phi_{\epsilon} = 2\pi \cdot \frac{I_{leak}}{I_{cp}} \quad [rad] \qquad (2.8)$$

Now if f_{REF} is the input reference frequency, f_{BW} is loop bandwidth, f_{pl} is the frequency of pole in loop filter and N is the division value then the amount of reference spur in 3rd order PLL is given by:

$$P_r = 20\log\left(\frac{1}{\sqrt{2}} \cdot \frac{f_{BW}}{f_{ref}} \cdot N \cdot \Phi_{\epsilon}\right) - 20\log\left(\frac{f_{ref}}{f_{pl}}\right) \quad [dBc] \qquad (2.9)$$

If reference spur is not enough to meet the requirement, the loop bandwidth should be further narrowed or charge pump current should be increased. It is also helpful to reduce the division value to relax the charge pump design.

2.5 Applications of PLL

Since its invention, PLL continues to find new applications in electronics, communication and instrumentation. Examples include memories, microprocessors, hard disk drive electronics, RF and wireless transceivers, clock recovery circuits on microcontroller boards and optical fibre receivers. Some of the applications are as follows [4].

Frequency multiplication and synthesis

A PLL can be modified such that it multiplies its input frequency by factor of M. Figure 2.7 shows basic frequency multiplication concept.

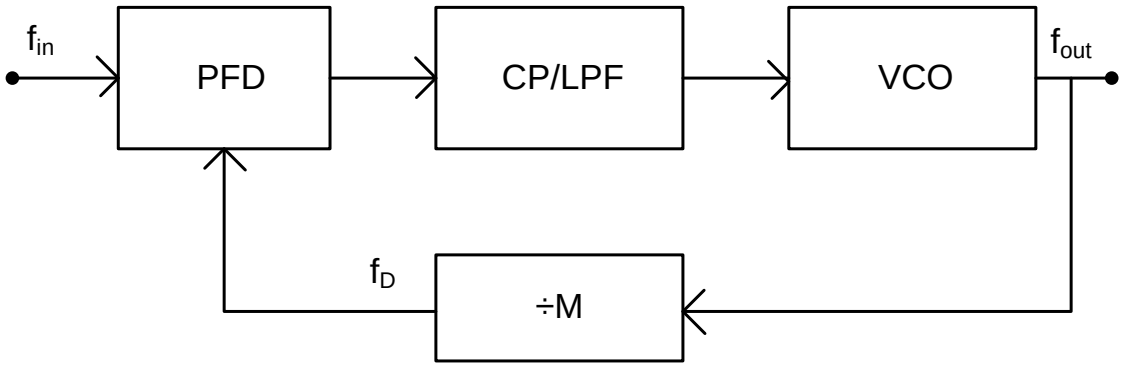

Fig. 2.7 Frequency Multiplication

Just like a voltage divider is used in feedback in voltage amplifier, as shown in figure 2.7, output frequency of PLL is divided by *M* and applied to the phase detector, we get, $f_{out}=M\,f_{in}$. Also, since f_{in} and f_D must be equal, PLL multiplies f_{in} by M.

Some systems require a periodic waveform whose frequency (a) must be very accurate and (b) can be varied in very fine stapes. Hence to synthesise a required frequency, a channel control word (digital) is applied to divider block in feedback that varies the value of M. Since f_{out}= M f_{REF}, the relative accuracy of f_{out} is equal to that of f_{REF}. It is also notable that f_{out} varies in stapes equal to f_{REF} if M changes by one each time.

Skew reduction

This is one of the very popular and earliest uses of PLL. Suppose synchronous pair of data and clock lines enter a large digital chip. Since clock typically drives a large number of transistors and logic interconnects, it is first applied to large buffer. Thus, the clock distributed on chip may suffer from substantial skew (delay due to buffer insertion) with respect to data. This is an undesirable effect which reduces the timing budget for on-chip operations.

Now consider the circuit as shown in figure 2.8. Here input clock CK_{in} is applied to on chip PLL and buffer is placed inside the loop. Since PLL guarantees a nominally zero phase

difference between CK_{in} and C_{KB}, the skew is eliminated. That is, the constant phase shift introduced by the buffer is divided by infinite loop gain of the feedback system. Alignment of V_{VCO} with CK_{in} is not important since V_{VCO} is not used.

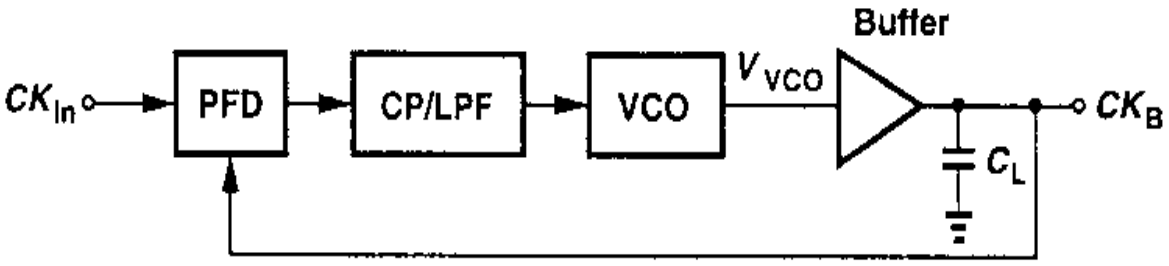

Fig 2.8 Use of PLL to Eliminate Skew.

Chapter 3

Charge Pump PLL

3.1 Introduction

Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO. Before arriving at the concept of charge pump, the problem of simple PLL which uses phase detector is discussed here.

Limitations of Simple PLL architecture

For type I PLL there are always trade-offs between damping ratio of loop filter, loop filter bandwidth and the phase error. Hence the performance of PLL cannot improve beyond certain limit. Apart from this, a simple PLL suffers from a critical drawback i.e. limited acquisition range [4]

Suppose when a PLL circuit is turned on, its oscillator operates at a frequency far from the input frequency, i.e., the loop is not locked. Now PLL starts acquiring a lock. The transition of the loop from unlocked to locked condition is very nonlinear process because phase detector senses unequal frequency. Also for this kind of PLL, the "acquisition range" is on the order of ω_{LPF}, that is, the loop locks only if the difference between ω_{in} and ω_{out} is less than roughly ω_{LPF}. If ω_{LPF} is reduces to suppress the ripple on control voltage, the acquisition range decreases. Even if the input frequency has a precisely controlled value, a wide acquisition range is often necessary because the VCO frequency may vary considerably with the process and temperature.

Hence in order to remove this problem, frequency detection is also incorporated in addition to phase detection. The concept is such that let the two frequencies (reference and VCO output frequency) be equal, once these two frequencies are equal, phases are compared and VCO is tuned such that phases of reference and feedback waveform are equal. Frequencies are compared using frequency detector which generates a dc voltage equal to the difference of two input frequency and drives the VCO such that $\omega_{in} = \omega_{out}$. When $|\omega_{in} - \omega_{out}|$ is

sufficiently small, phase locked loop takes over, acquiring lock. Such scheme increases the acquisition range to the tuning range of VCO.

3.2 Phase frequency detector

For the periodic signal it is possible to merge the phase and frequency detector, such that it can detect both phase and frequency. It is called as phase-frequency detector (PFD) [4] [8] and illustrated conceptually in figure 3.1.

Suppose two waveforms A and B arrive at input pins with equal frequency but unequal phases such that A leads B. As A goes high, output Q_A goes high. When leading edge of B comes, Q_A goes to zero while Q_B does not show any change and remains low. Exactly opposite thing happens when B leads A. Thus output QA continues to produce pulses whose width is proportional to $|\Phi_A - \Phi_B|$ while Q_B remains at zero. Now as shown in figure 3.1(b), suppose A has higher frequency than B and also A leads B, then Q_A continues to produce the pulses with unequal width and Q_B remains quite and vice versa. Thus, the dc contents of Q_A and Q_B provide information about phase or frequency difference. Outputs Q_A and Q_B are called the "UP" and "DOWN" pulses, respectively.

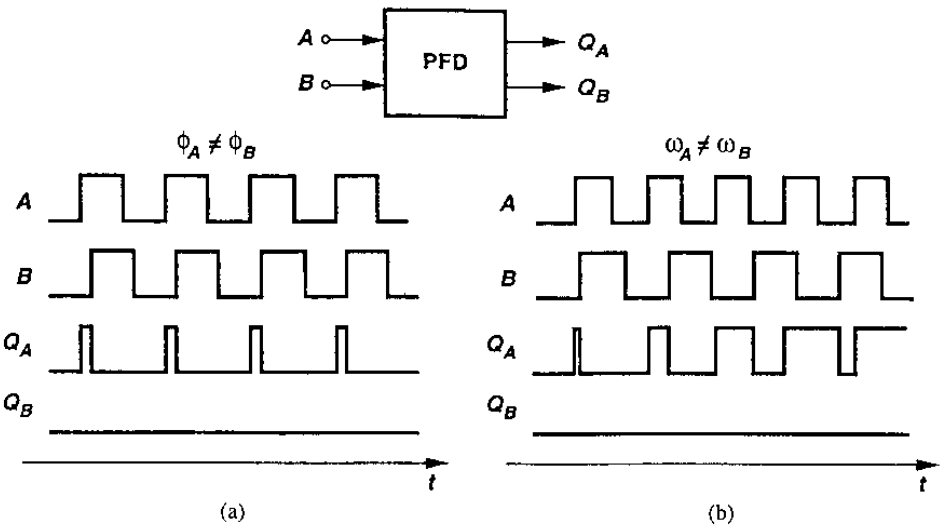

Fig. 3.1 Concept of Phase Frequency Detector (PFD)

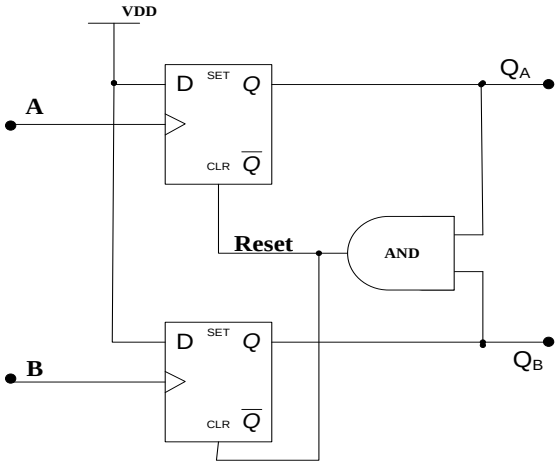

Fig. 3.2 Implementation of PFD

Figure 3.2 shows the implementation of PFD. It consists of two edge triggered resettable D flipflops with their D inputs tied to logical ONE. Inputs A and B serve as clock of flipflops. If QA=QB=0 and A goes high, QA rises. If this event is followed by a rising transition on B, QB also goes high and the AND gate resets both flipflops. In other words, QA and QB are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly. Figure 3.3 shows the operation of phase frequency detector.

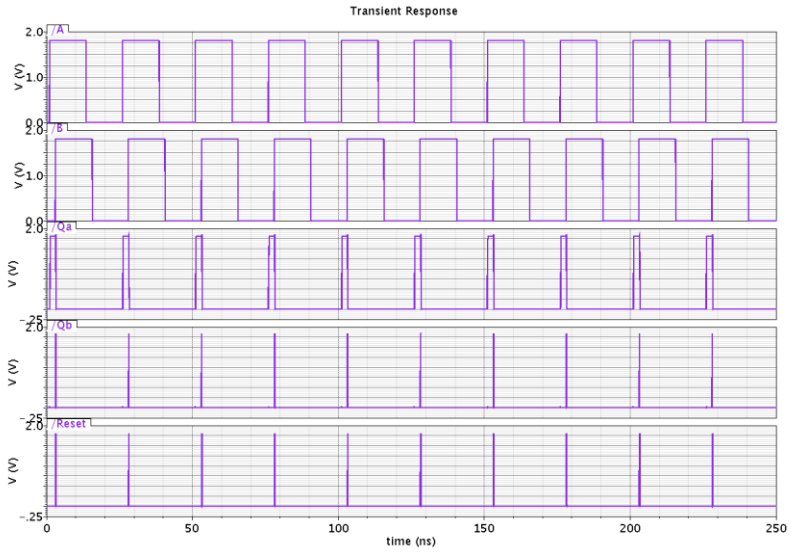

Fig. 3.3 PFD Response

It is just seen, that PFD effectively converts the input phase or frequency difference information into the proportional UP and DOWN pulses. But, how to utilise this information to generate a voltage which is used to the VCO? Since the difference between the average values of QA and QB is of interest, the two outputs can be low pass filtered and sensed differentially. However a more common approach is to interpose a "CHARGE PUMP" between PFD and LPF.

3.3 The Charge Pump

A charge pump [4] [9] is a three position electronic switch which is controlled by the three states of PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm V_P$ or a pump current $\pm I_P$ to the loop filter. When both UP and DOWN of PFD are off, i.e. N position, the switch is open, thus isolating the loop filter from the charge pump and PFD. Figure 3.4 shows the basic charge pump.

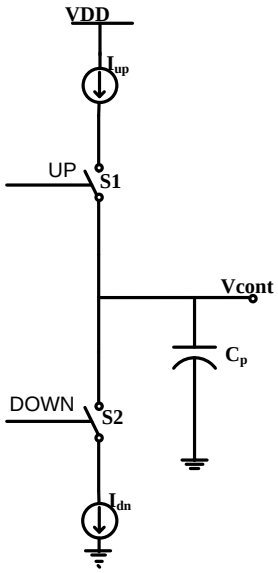

Fig. 3.4 Basic Charge Pump Architecture.

Figure 3.4 shows the combined architecture of the charge pump and loop filter. Current sources I_{up} and I_{dn} are identical. Two outputs of PFD Q_A and Q_B are given to the UP and DOWN inputs of charge pump (CP) respectively. Capacitor C_p serves the purpose of loop filter. Figure 3.5 shows the CP accompanied with PFD and loop filter.

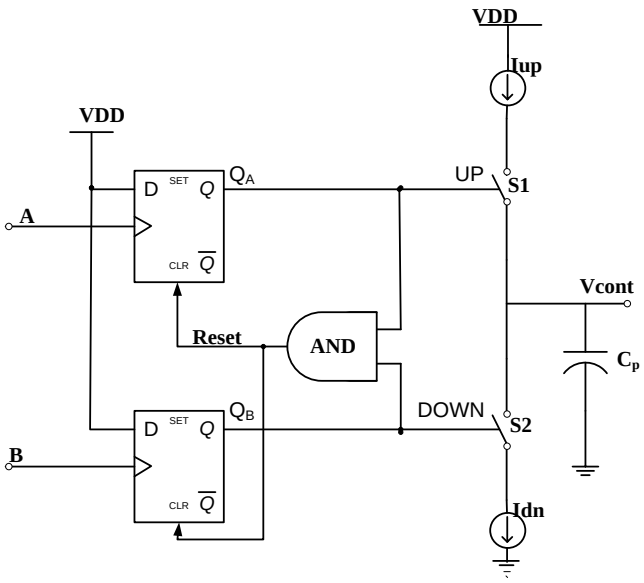

Fig. 3.5 PFD-CP-Loop Filter Combination

If Q_A=Q_B=0, then S1 and S2 are off and V_{out} (or V_{cont}) remains constant. If Q_A is high and Q_B is low, then I_{up} (UP current) charges C_p. Conversely if Q_A is low and Q_B is high, then I_{dn} (DOWN current) discharges C_p. Hence, if suppose, A leads B, then Q_A continues to produce pulses and V_{cont} rises steadily. Figure 3.6 shows the response of PFD-CP combination.

Fig. 3.6 Response of PFD-CP combination

3.4 Theory of Basic Charge Pump PLL

The basic PLL using charge pump PLL [4] is discussed here. Figure 3.7 shows such construction.

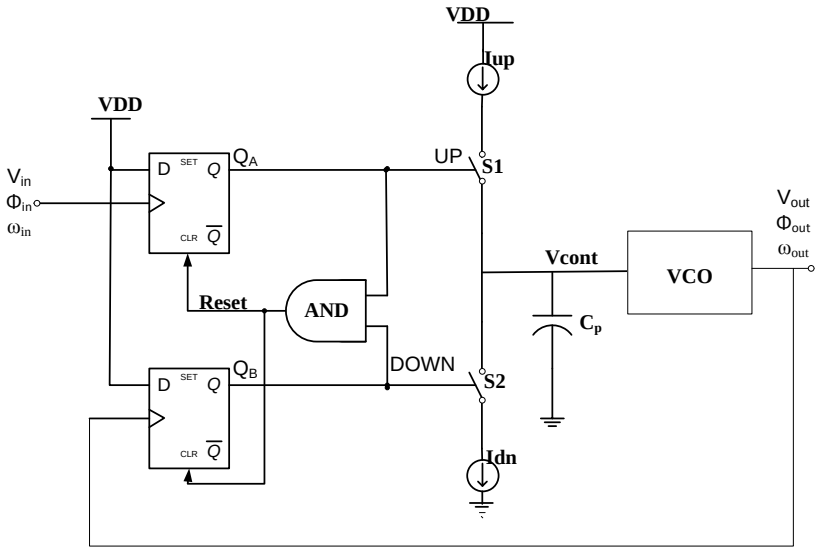

Fig. 3.7 Simple Charge Pump PLL

The reference input is given to the one of the PFD while VCO output is given to another input. This implementation senses the transition at the input and output detects phase or frequency difference and activates the charge pump accordingly. When loop is turned on, ω_{out} may be far ω_{in}, and the PFD and charge pump vary the control voltage such that ω_{out} approaches ω_{in}. When input and output frequencies are sufficiently close, the PFD operates as phase detector, performing phase lock.

Now consider a case, that $\Phi_{out} - \Phi_{in}$ drops to zero. In this case PFD simply produce $Q_A = Q_B = 0$. The charge pump thus remains idle and Cp sustains a constant control voltage. But this does not mean that PFD and CP are no longer needed. If V_{cont} remains constant for a long time, the VCO frequency and phase begin to drift. In particular, the VCO create random variations in the oscillation frequency that can result in large accumulation of phase error. The PFD then detects the phase difference, produces corrective pulses on Q_A or Q_B that

adjusts the VCO frequency through charge pump and filter. Also, as phase comparison is performed in every cycle, the VCO phase and frequency cannot drift substantially.

Let`s construct the mathematical model for simple CP-PLL.

Let the two different signals arriving at A and B have equal frequency but unequal phase. Let T_{ref} is time period of reference input and Δt is the time difference between signal A and signal B. The phase difference (or phase error) between two input signals is given by:

$$\Delta\Phi = \frac{\Delta t}{T_{ref}} \qquad (3.1)$$

The phase difference is zero when loop is locked. Hence referring the Fig. 2.2, the output voltage of PFD is given by:

$$V_{PFD} = \frac{VDD-0}{4\pi} \cdot \Delta\Phi \qquad (3.2)$$

Hence the gain of PFD is given by:

$$K_{PFD} = \frac{VDD}{4\pi} \quad [volts/rad] \qquad (3.3)$$

The output of the PFD is then given to the charge pump. The operation of which is already described in section 3.2. Referring to this discussion we say that the characteristic of I_P (charge pump current, Up or Down) is of Signam function $I_P = I_P \, sgn(\Delta\Phi)$. That is, I_P is $+I_P$ if ΔΦ is positive and Ip is $-I_P$ if this phase error is negative. Now in locked condition of PLL, the ON time of UP or DOWN switch is given by:

$$t_p = \frac{\Delta\Phi}{2\pi f_{in}} \text{ s} \qquad (3.4)$$

Then the current delivered to the filter C_p for the time t_p on each cycle is given by:

$$I_d = \frac{I_P - (-I_P)}{4\pi} \cdot \Delta\Phi \tag{3.5}$$

$$\Rightarrow K_{PFD} = \frac{I_P}{2\pi} \tag{3.6}$$

Thus the control voltage generated across the CP is given by:

$$V_c(s) = \frac{I_d(s)}{Z_c(s)} = \frac{I_P}{2\pi} \cdot \frac{1}{Z_c(s)} \cdot \Delta\Phi = K_{PFD-CP} \cdot \Delta\Phi \tag{3.7}$$

$$\Rightarrow K_{PFD-CP} = \frac{I_P}{2\pi C_p} \ [Volts/rad] \tag{3.8}$$

Now suppose in a locked condition, suddenly $\Delta\Phi = \Delta\Phi_o\, u(t)$ phase difference is introduced. Q_A will produce the pulses which are $\Delta t = \Delta\Phi \cdot T/2\pi$ sec wide which leads to output to rise by $(I_P/C_P) \cdot (T/2\pi) \cdot (\Delta\Phi)$ in every period. Approximating this to a ramp voltage we can write:

$$V_c(t) = \frac{I_P}{2\pi C_p} \cdot \Delta\Phi \cdot t \cdot u(t) \tag{3.9}$$

This leads to impulse response:

$$h(t) = \frac{I_P}{2\pi C_p} \cdot u(t) \tag{3.10}$$

Hence the transfer function of PFD-CP-Filter combination is given by:

$$\frac{V_{cont}}{\Delta\Phi}(s) = \frac{I_P}{2\pi C_p} \cdot \frac{1}{s} \tag{3.11}$$

This output of PFD-CP-Filter combination is then given to the VCO with transfer function as (K_{VCO}/s). Hence referring the model given in section 2.1 with Figure 2.4 we can write the open loop transfer function of simple Charge Pump PLL as:

$$\frac{\Phi_{out}}{\Phi_{in}}(s)|_{open} = \frac{I_P}{2\pi C_p} \cdot \frac{K_{VCO}}{s^2} \tag{3.12}$$

Since the open loop gain has two poles at origin, this topology is called as "type II" PLL. The closed loop transfer function is given by:

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_p}}{s^2 + \frac{I_P K_{VCO}}{2\pi C_p}} \tag{3.13}$$

This result is alarming, because closed loop system contains two imaginary poles and therefore unstable. In order to stabilise the system, we add a zero in the loop gain by adding a resistor R_p in series with the loop filter capacitor. This system is shown in figure 3.7 with additional capacitor C_2 whose purpose will be explained later.

The PFD-CP-Filter now has the transfer function:

$$\frac{V_{cont}}{\Delta\Phi}(s) = \frac{I_P}{2\pi}\left(R_p + \frac{1}{C_p s}\right) \tag{3.14}$$

Thus the closed loop transfer function of this system becomes:

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_p}(R_p c_p \cdot s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO}\, R_p \cdot s + \frac{I_P}{2\pi C_p} K_{VCO}} \tag{3.15}$$

The closed loop system contains a zero at $s_z = -1/(R_p C_p)$. The natural frequency and the damping ratio are given as:

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_p}} \tag{3.16}$$

$$\zeta = \frac{R_p}{2}\sqrt{\frac{I_P C_p K_{VCO}}{2\pi}} \tag{3.17}$$

As expected, if R_p=0, then ζ =0. With complex poles, the decay time constant is given by $1/(\zeta\,\omega_n) = 4\pi/(R_p I_P K_{VCO})$.

As seen from the equation 3.15 if we decrease the $I_P \cdot K_{VCO}$, the gain crossover frequency decreases (or shifts toward the origin), degrading the phase margin.

But this compensated type PLL suffers from a drawback. Since the charge pump drives the series combination of R_p and C_p, each time a current is injected into the loop filter, the control voltage experiences a large jump. Even in the locked condition, mismatches between I_{up} and I_{down} and the charge pump injection and clock feed through of S_1 and S_2 introduce voltage jump in V_{cont}.

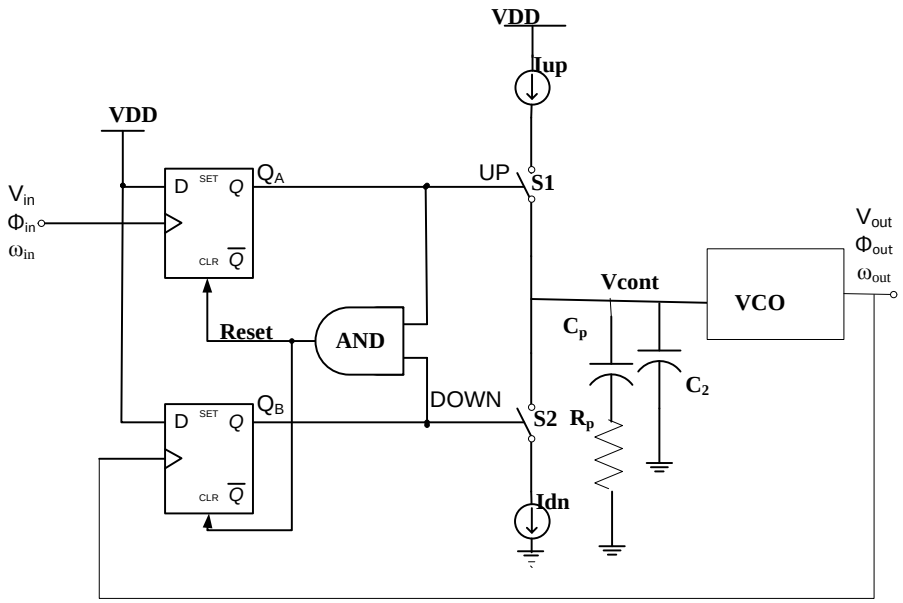

Fig. 3.8 Addition of R_P and C_2 to Improve Stability

The resulting ripple severely disturbs the VCO, corrupting the output phase. To solve this problem, a second capacitor C_2 is usually added in parallel with R_p and C_p, suppressing the initial step. The loop filter is now of second order, yielding a PLL of type III. Generally C_2 if about one-fifth to one-tenth of C_p and does not affect the closed loop time and frequency response. Figure 3.8 shows the third order PLL construction.

3.5 Voltage Controlled Oscillator

Voltage controlled oscillator [10] is one of the important elements of PLL. Since, here our aim is to study charge pump, without going into the details of VCO theory, its parameters used in design, are directly given.

VCO type: Current Starved 5 stage VCO

Range of VCO: 170 KHz to 170 MHz approximately.

Central frequency: 110 MHz

VCO gain: 333.95 MHz/V for the range 0.7 V to 0.9V

103.707 MHz/V for the range 0.2 V to 1.8V

Central frequency bias current: 60 µA.

W/L ratios: M6, M4, M10…: 0.4µ /3µ

M3, M9…: 1.2µ/0.1µ

M2, M8…: 0.6µ/0.1µ

M5, M1, M7….: 0.4µ/2µ

Figure 3.9 shows the circuit diagram and Figure 3.10 shows the characteristics of VCO

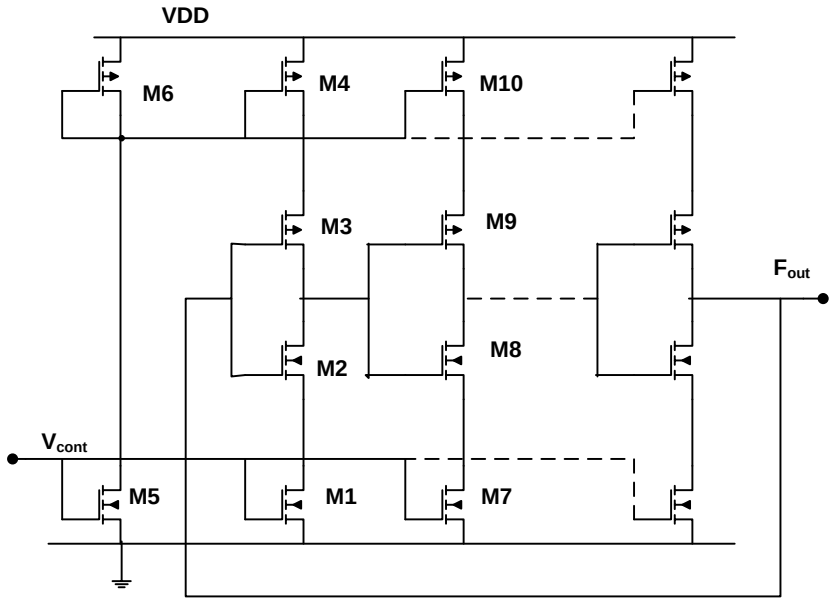

Fig. 3.9 Current starved VCO

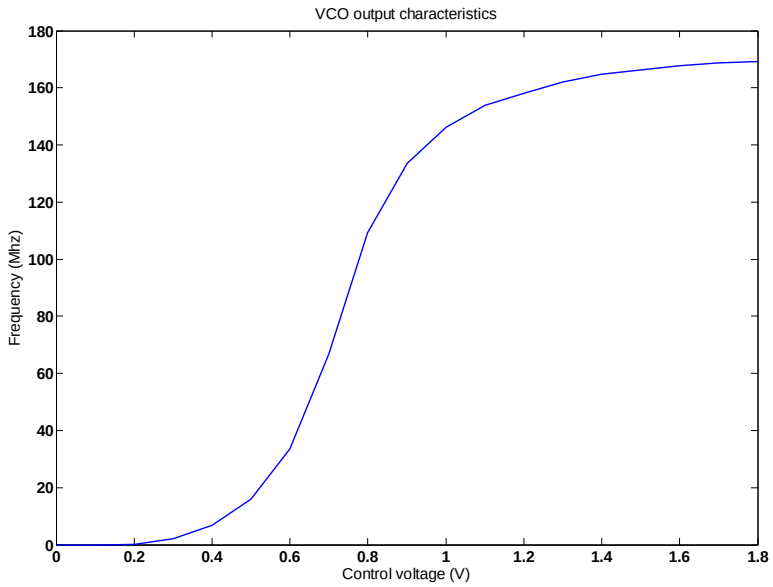

Fig. 3.10 VCO characteristics

3.6 Basic Charge Pump

The properties and problems related to charge pump architectures are discussed here. It is well known that a transistor biased with a constant voltage in saturation, works as constant current source. Also a MOSFET can work as a high speed switch. Using these basic concepts, the basic charge pump constructed is shown in figure 3.11.

As shown in figure 3.11, switch S_1 is implemented using PMOS M3 while UP current source is implemented using the fixed biased M4. Similarly for discharging circuit M2 serves as switch S_2 and M1 serves as DOWN current source. Inverter is inserted so that M3 will be on when Q_A is high. But insertion of inverter introduces a delay in path thereby introducing a skew between Q_A and Q_B. To eliminate this effect, a pass transistor gate is inserted between QB and M2. Hence delays of inverter and pass transistor gate become equal.

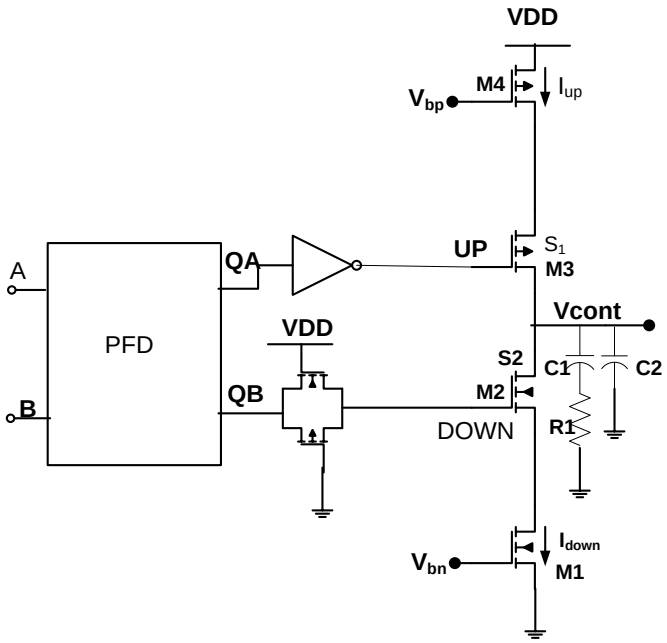

Fig. 3.11 Implementation of Basic Charge Pump

3.6.1 Simulation Studies

All circuits in this work are implemented using "Cadence" tool in "Virtuoso Analog Design Environment". The library used is GPDK090 with 100nm technology. All the circuits are simulated using "Spectre" simulator tool. The voltage supply used is 1.8V. Reference frequency is kept at 40MHz and simulation is run for 10µs.

3.6.2 Results and Discussion

The PLL is implemented using the basic charge pump shown in figure 3.11. The simulation is run for 10µs transient time period. Figure 3.12 shows the transient response of basic charge pump PLL while figure 3.13 shows the time verses frequency response of PLL. As seen in figure 3.12, the output frequency of PLL is initially away from the reference input frequency. The PFD then produces the pulses, such that CP-LPF combination drives the VCO towards the reference input frequency. Control voltage starts increasing and once the loop is locked, it remains relatively stable. As discussed earlier, this transition is nonlinear

phenomenon which is clearly seen in figure 3.13. It can also be seen that the loop is locked at 20MHz instead of 40MHz, which it should. Causes of this behaviour will be discussed in the next section. To conclude, we say that the basic charge pump and PLL is implemented using the Cadence tool and simulation is run. PLL is in fact failed to acquire a lock. The power consumption is found as 0.1751mW and current mismatch is found to be around 76µA. The value of reference spur is found to be -32.6155 dBc.

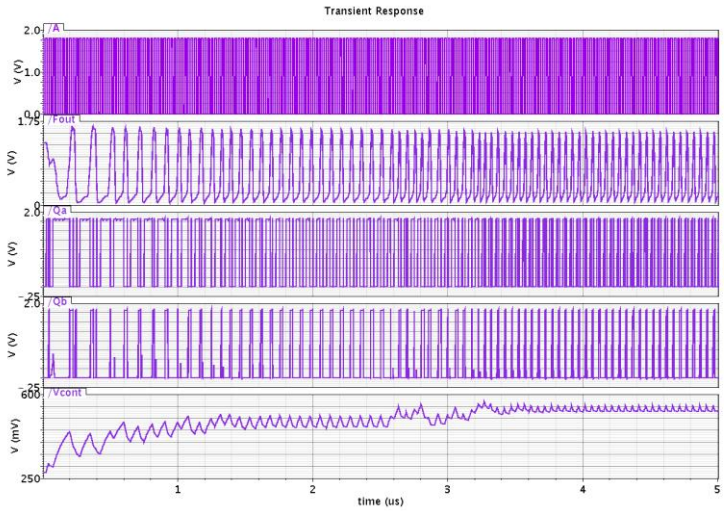

Fig. 3.12 Transient Response of Basic Charge Pump PLL

Fig. 3.13 Time Verses Frequency Response of Basic CP-PLL

3.7 Non Ideal Effects in Charge Pump

If observed carefully in Fig. 3.12, it is clear that, PLL is locking at 20MHz rather than at 40MHz, which it should. Why is it happening? This is the result of non ideal effects in CP [4] [11]. This issue discussed below.

1. As shown in Fig. 3.11 switches are constructed using PMOS and NMOS. The inherent mismatches between these two switches results in mismatch in charging and discharging current in addition to timing mismatch. Hence there is variation in control voltage at the output. In fact the W/L ratios are adjusted so as to have equal UP and DOWN currents. Even though, about 73μA mismatching is observed between these currents in simulation. That means, since two current sources are themselves mismatched, the control voltage experiences the random changes in it.
2. There is also problem of charge sharing between output node of CP (in fact between filter capacitor) and the parasitic capacitances between drain and source of switch transistors. This results in sudden change in control voltage which may disturb the VCO.
3. Another effect is clock feed through. The high frequency signal provided at the gate of switch transistor passes to the output node via gate to drain parasitic capacitor C_{gd}. This also results in jumps in control voltage. Since the VCO sensitivity is high, even a small jump in control voltage results a large jump in output frequency.

   If we observe the control voltage in figure 3.12, after roughly 3.5μs loop stabilizes. Though control voltage is relatively stable, there are small jumps in it which can be clearly seen in the transient response. This is the effect of clock feed through as well as charge sharing. The result is sudden jump in output frequency which we can see in the figure 3.13 after 4μs approximately.

4. Another effect is limited output voltage. If we want higher output voltage the current source value must be increased. This is not possible in every condition, since that increases power consumption also. In fig. 3.12, control voltage rises only up to some 550mV, but desired value is around 632mV for 40MHz. Hence PLL fails to acquire the lock.

Apart from this reference spur in PLL is also one of the critical problem which arises due to current mismatches in charge pump. Referring to the section 2.4 (c) of reference spur, equation 2.8 can be modified as:

$$|\Phi_\epsilon| = 2\pi \cdot \frac{\Delta t_{on}}{T_{ref}} \cdot \frac{\Delta i}{I} \qquad (3.18)$$

Where Δt_{on} is turn on time of PFD, T_{ref} is reference time period, Δi is charge pump current mismatch and I is charge pump current. The equation 2.9 remains unchanged.

To remove the non ideal effects in CP, so many different architectures are proposed. In practice charge pumps are roughly classified into two categories. “Single ended charge pump” and “Differential charge pump”.

3.8 Single Ended and Differential Charge Pumps

In single ended charge pump [11] only two inputs UP and DOWN are given to the respective switches, while in differential charge pump two outputs of PFD are given to the two differential switches with each input inverted and given to the second input of the respective switch[11]. Figure 3.14 shows one of the examples of differential charge pump.

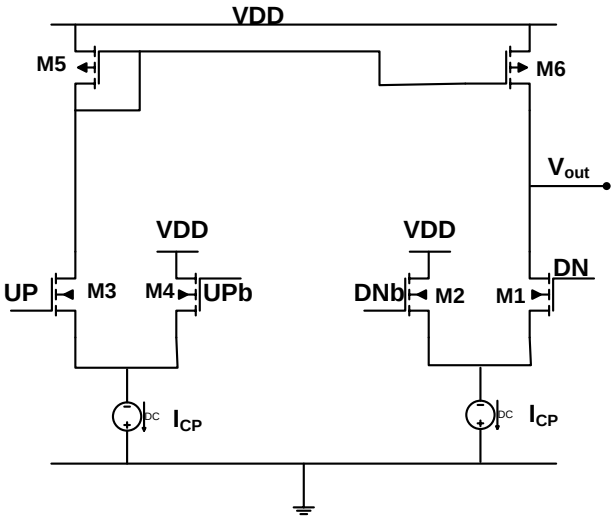

Fig. 3.14 Example of Differential Charge Pump

Without going into the details of differential charge pump, the advantages and limitations of differential charge pump are listed below.

3.8.1 Advantages of Differential Charge Pumps

1. The switching mismatch between NMOS and PMOS does not affect the overall performance substantially. The matching requirement between NMOS and PMOS transistors are relaxed to the matching between NMOS or between PMOS transistors respectively.
2. The differential CP uses switches using NMOS and the inverter delays for UPb and DNb signals do not generate any offset due to its fully symmetric operation.
3. This configuration doubles the range of output voltage compliance compared to single ended charge pump.
4. Differential stage is less sensitive to the leakage current since leakage current behaves as common mode offset with the dual output stages.

3.8.2 Limitations of Differential Charge Pumps

Though differential CP has many advantages listed above, they suffer from critical drawbacks. They require two loop filters and common mode feedback circuitry. Since more number of transistors are required, with two or more current sources, they occupy large silicon area. This also leads to higher power consumption.

3.8.3 Limitations of Single Ended Charge Pumps

1. Switch mismatch, clock feed through, charge sharing problems are still not eliminated fully.

2. Limited output voltage compliance range. For source CP shown above if we want higher output voltage we have to increase the charging and discharging current values.

3. Switch mismatch also results in timing mismatch as well as dead zone.

4. Parasitic capacitances are dominant in single ended CP. Using of OPAmp may solve above mentioned problems; but designing of OPAmp it itself tedious process and also increases unnecessary hardware.

Even though single ended charge pump has these disadvantages, they are more popular than differential design, because they do don't require two loop filter and offer tri state operation with lower power consumption. Also the problems listed above are not those much difficult to handle. With proper modification into the architecture, these problems can be eliminated or minimised easily. Also, single ended charge pumps require fewer components than differential charge pumps; hence they occupy less area in a chip. In the next session we will discuss the different architectures of single ended charge pumps with their simulation and comparison.

3.9 Analysis Different Single Ended Charge Pump Architectures

To remove the non ideal effects in basic charge pump as well as in single ended charge pump many topologies are proposed. Here we will discuss two topologies among them which briefly cover all required aspects of charge pump.

3.9.1 Source Charge Pump

Figure 3.15 shows the source charge pump [11]. The topology uses simple current mirrors to generate charging and discharging current from two identical current sources. Switches are placed at the source of current mirror MOS transistor as shown in figure.

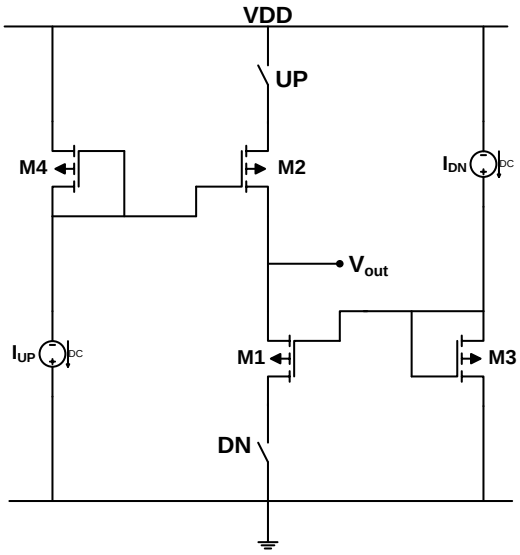

Fig. 3.15 Source Charge Pump

The advantage of this kind of topology is that, transistors M1 and M2 are always guaranteed to be in saturation, since combinations M1-M3 and M2-M4 form the current mirrors. The g_m (transconductance) of M3 and M4 does not affect the switching time. This architecture gives the faster switching time than other topologies in which switches are implemented at the drain or gate terminals of the transistors; since the switch is connected to single transistor with lower parasitic capacitance.

a. *Design of current mirrors for source CP*

The gate terminal of both M3 and M4 are tied to their respective drain terminal. Hence these two transistors go into hard saturation. Here we use the principle that, if gate source potentials of two identical MOS transistors are equal, the channel currents should be equal. Now, $V_{DS3}= V_{GS3}= V_{GS1}$, (assuming negligible switch resistance). Thus from circuit, neglecting channel length modulation, we can write that:

$$I_{DN} = \frac{k_3' W_3}{2L_3}(V_{GS3} - V_T)^2 = I_{D1} = \frac{k_1' W_1}{2L_1}(V_{GS1} - V_T)^2 \tag{3.19}$$

Since transistors are identical, hence we can write that:

$$\frac{I_{DN}}{I_{D1}} = \left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{3.20}$$

By similar ideology we can write that:

$$\frac{I_{UP}}{I_{D2}} = \left(\frac{W_4/L_4}{W_2/L_2}\right) \tag{3.21}$$

The small signal output resistance is given as:

$$r_{out} = \frac{1}{g_{ds}} \tag{3.22}$$

From equation 3.22 it is clear that simple current mirror exhibits poor output resistance.

b. *Simulation results*

Simulation is performed for source charge pump in Spectre simulator. Reference input frequency is kept at 40MHz. Figure 3.16 shows the transient response while figure 3.17 shows the time verses frequency response of source CP-PLL

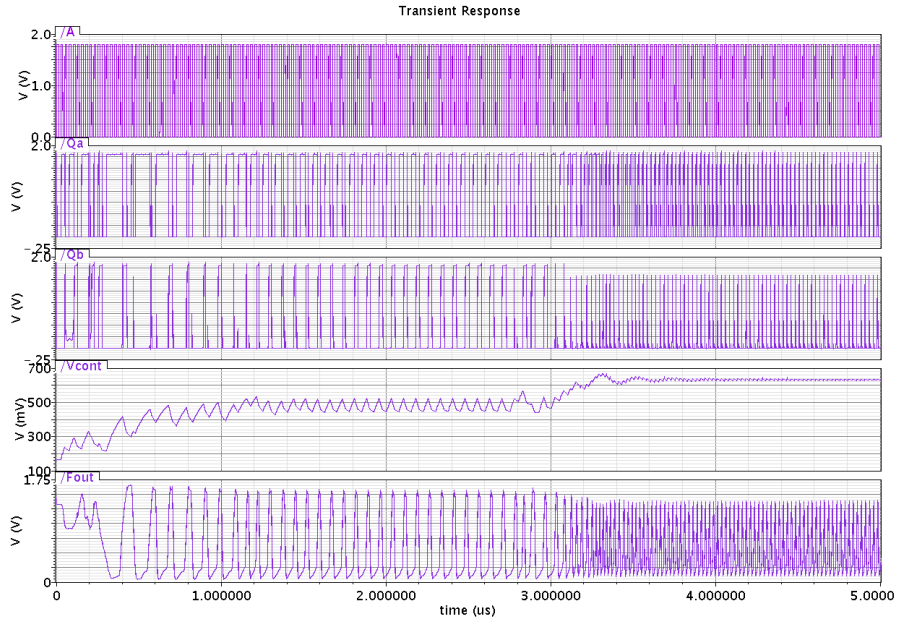

Fig. 3.16 Transient Response of Source CP-PLL

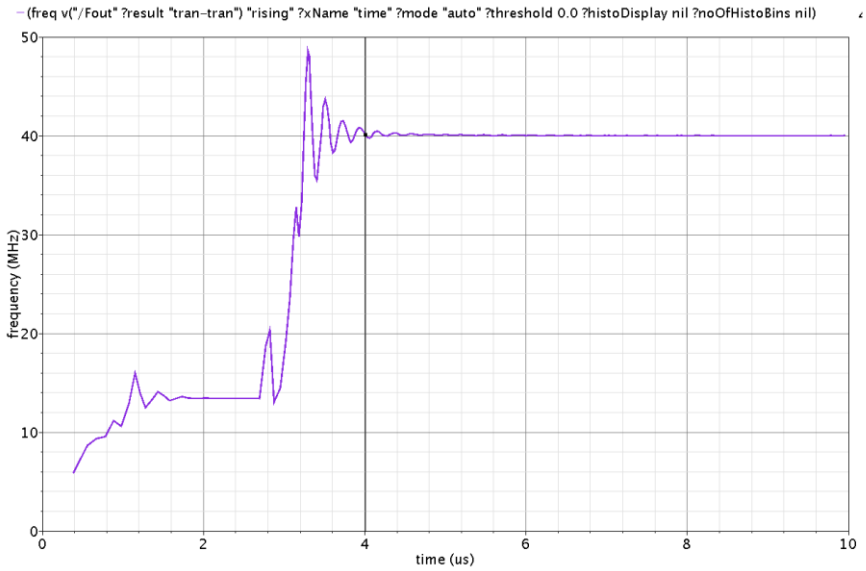

Fig. 3.17 Time Verses Frequency Response of Source CP-PLL

c. Discussions

a. If figure 3.16 is carefully observed, it will be seen that the ripples in the control voltage in the locked state of PLL are drastically reduced.

b. Also CP builds enough voltage (632 mV in fact) to tune the VCO to the reference input frequency.

c. Loop roughly locks into 4µs.

d. The power consumption was found to be 1.9896 mW, which is quite higher. The bias current requirement is found to be 500µA.

e. Mismatch in UP and DOWN currents is found to be 70µA. The reference spur value is found to be -61.288 dBc.

d. Limitations of Source CP

a. The simple current mirror used in this topology has low output impedance. To have output current constant over a supply range the output impedance of current mirror must be high.

b. Also it is observed that, if we want optimum output voltage across the CP as well as optimum pull in time of PLL, the bias current requirement is also high (500µA current is required here).

c. Two current sources are required here, which add further power consumption, because large number of transistors are required building a constant current source.

d. The mismatch between PMOS and NMOS is not fully removed. Also the clock feed through effect is not minimised fully.

Considering all these limitations, in next section we will consider a new topology in which these limitations are tried to remove.

3.9.2 Transmission Gate Charge Pump

Many architectures were proposed to reduce the non ideal effects in charge pump. Transmission gate charge pump is one of such proposed topology. Following points were considered while designing this topology.

1. If we derive both UP and DOWN current from same current source, the inherent current mismatch can be minimised. This also removes requirement of two current sources, hence also reduces power consumption.
2. Use of high output impedance current mirror, so that there is no variation in charging and discharging currents.
3. If we use transmission gate switches instead of normal NMOS or PMOS switches, switching time will increase as well as we can remove switching mismatch.

Figure 3.18 shows the Transmission Gate CP topology [12].

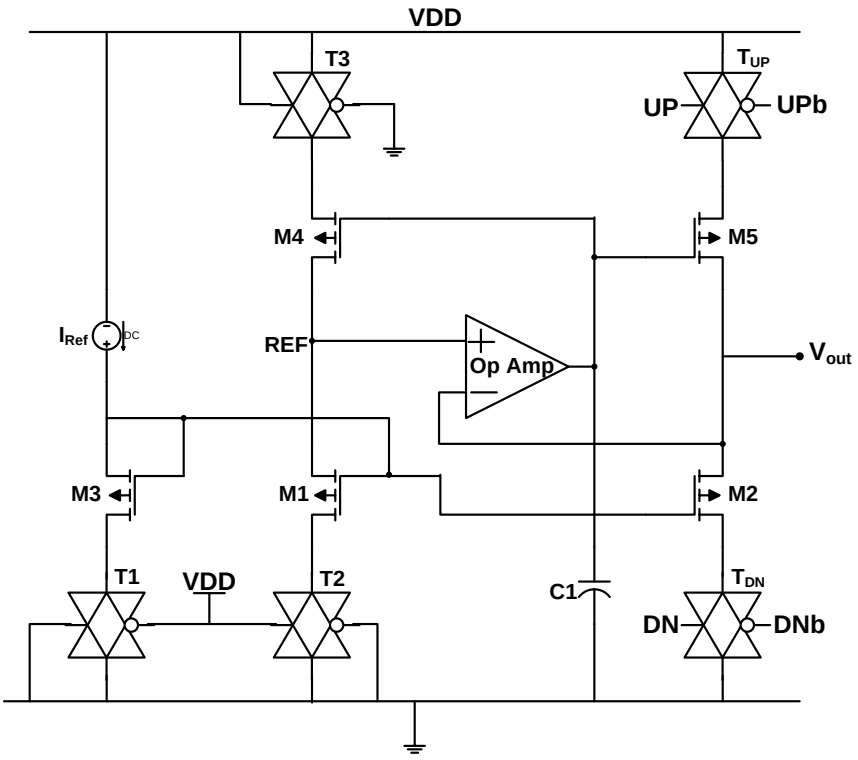

Fig. 3.18 Transmission Gate Charge Pump (TGCP)

The figure 3.18 shown is obviously the source charge pump but with modifications for reducing the non ideal effects. This topology tries to bring the advantages of differential charge pumps. The switches in this circuit are implemented using transmission gates (TG) which are driven by complementary clock signals. The usage of TG almost eliminates the

clock feed through. Both UP and DOWN currents are derived from same reference current source (20 μA) via current mirrors. So, it can avoid the current mismatch caused by the case in which these two currents are derived from two different sources. The high gain folded cascode operational amplifier (OP Amp) is added to CP to make the voltage V_{REF} at REF node, to follow the voltage V_C (voltage at output node or across capacitor) at the output of the CP branch. In other words, OP Amp and Current mirror combination forms the regulated input current mirror in which the V_{DS} of current mirrors are forced to be the same, which makes CP immune to channel length modulation effects. To shun the current mirror mismatch caused by inserting T_{UP} and T_{DN}, T1, T2 and T3 are inserted into the circuit. A large bypass capacitor C_1 is added to the charge pump to further attenuate the glitches since it provide additional path to the ground.

a. Design and simulation results

The sizes of transistors and gates should be properly adjusted to maximise the effective output voltage range, to expand the tuning range of CP-PLL, to minimise the turn on time of PFD to reduce the in band noise contribution of the PLL to the output. The required reference current IREF is found to be only 20μA. The W/L of M3 and T1 is equal to that of M1 and T2 respectively. But W/L of T3, M4, M1 and T2 are 3 times of that T_{UP}, M5, M2 and T_{DN} respectively. The specifications of folded cascode OP Amp are as follows:

Slew Rate: 10 V/μs

C_L= 10 pF

V_{out}= ± 1.2 V

VDD= |-VSS|= 1.8V

GB= 10MHz

Minimum input common mode voltage: -1V

Maximum input common mode voltage: 1V

A_d= 5000 v/v

Figure 3.19 shows the transient response while figure 3.20 shows the times verses frequency response of TG CP-PLL.

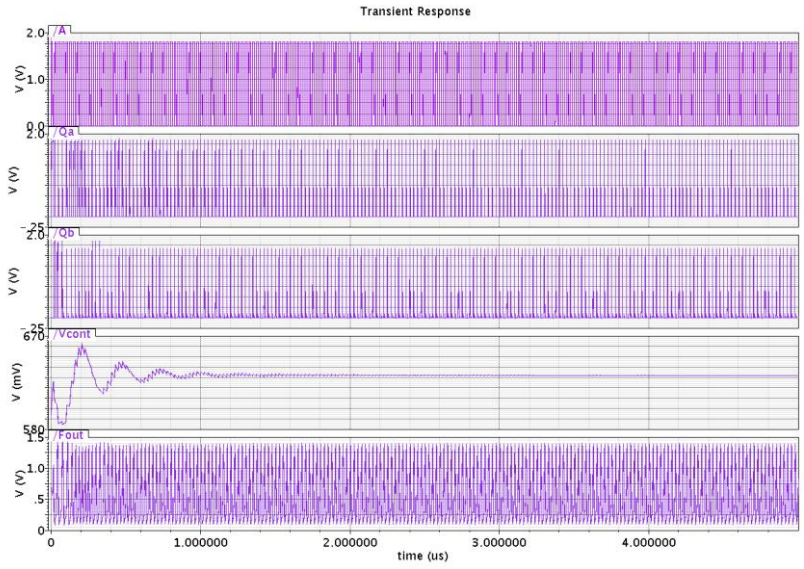

Fig. 3.19 Transient Response of TGCP-PLL

b. Discussion

a. No ripple in the control voltage after loop is locked. This can be seen clearly in figure 3.18 after approximately 3µs.

b. The pull in time is found as 1.2µs approximately which is well below the pull in time of source CP-PLL

c. Power consumption is found to be 1.298mW, which is less than source CP-PLL.

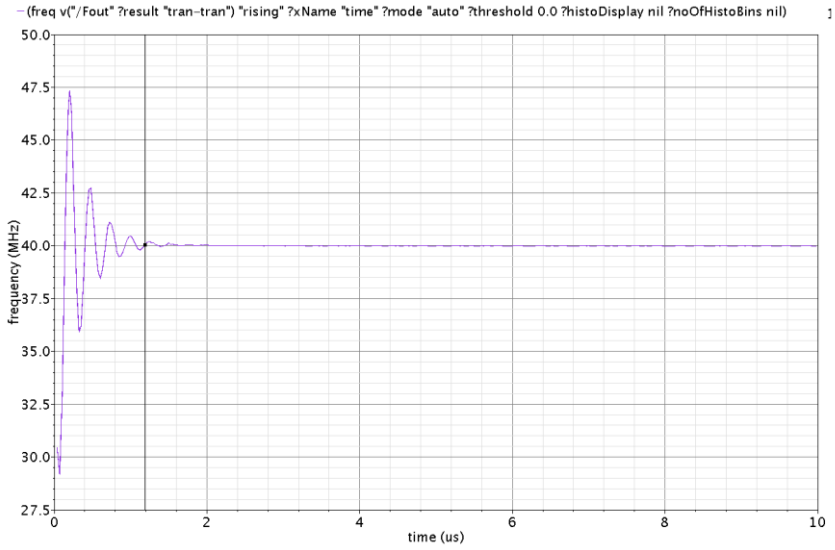

Fig. 3.20 Time Verses Frequency Response of TGCP-PLL

d. The current mismatch between UP and DOWN current found as 12µA only. The value of reference spur is found as -48.64 dBc.

c. Limitations

Though TG CP removes almost all non ideal effects in charge pump, certain limitations are found in this topology.

a. Though the pull in time of PLL is improved (reduced, as it is primary requirement), the power consumption has not reduced in that proportion.

b. The reason is that, this topology uses OP Amp, which contributes to the major power consumption of the circuit.

c. Further, design of OP Amp is itself tedious process. Hence if requirement of OP Amp are not met, total circuit malfunctions.

d. Considering efficiency, it is clear that this circuit consumes large area on silicon wafer since design of OP Amp needs resistors and capacitors which are major area consumption elements in chip. A large by pass capacitor used also consumes more area on chip.

e. The value of reference spur is higher than source CP reference spur. Hence we can say that relative to source CP`s noise performance is poor.

Considering these limitations, a new topology has been thought, which should have all advantages of TG-CP, but it should be more area efficient, fast as well as should consume less power than current topology. In the next chapter, proposed topology is discussed along with comparison with all topologies considered in this thesis.

Chapter 4

Novel CP Architecture

4.1 An Introduction to Self Biased High Swing Cascode Current Mirror

A new topology which will remove the disadvantages of TGCP at the same time retain its advantages is proposed here. The main component of any charge pump is the current mirror used in it. An efficient current mirror exhibits the following properties [13].

1. It has very high output impedance. Hence there will be very less variation in output current for small change in output voltage.
2. It has high output voltage compliance. That is the range of the voltage over which output current remains constant should be high.
3. It consumes less power.
4. It is immune to power supply variation as well as noise.

Many architectures of current mirrors are available in the literature e.g. Cascode current mirror, Wilson current mirror, High Swing Cascode current mirror and others. Some architectures use the OP Amp in their circuit, but as discussed earlier it unnecessarily increases hardware complexity. Considering many topologies in literature, it is decided to use "Self Biased High Swing Cascode Current Mirror" [14]. The reason behind this choice is in the advantages of this topology.

1. Very easy to design. Does not require extra current source for biasing.
2. Can work efficiently even if very less amount of bias current is provided.
3. Very high output impedance. (10MΩ approximately)
4. Good output voltage compliance.
5. Consumes very less power.
6. Suitable for working in sub 1V environment.

The self biased high swing cascode current mirror circuit is depicted in figure 4.1.

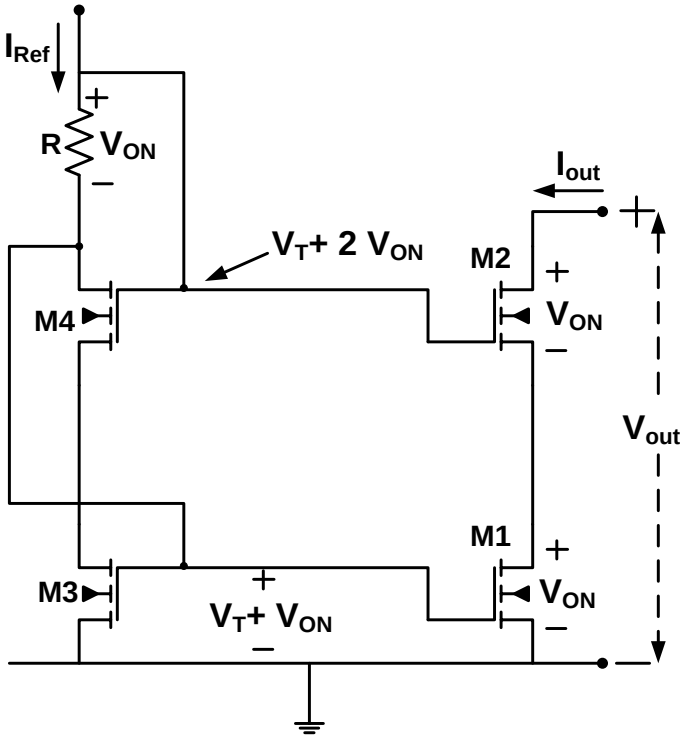

Fig. 4.1 Self Biased High Swing Cascode Current Mirror

As shown in figure 4.1, a resistor R is used to create the bias by dividing the voltage across it. All the transistors are in saturation. The W/L values of M1 and M3 are calculated using the normal drain current formula of MOSFET in saturation. The gates of M2 and M4 are get back biased by V_{ON} (here bulks of all transistors are grounded). Hence the threshold voltages for M2 and M4 can be calculated as:

$$V_{T4,2} = V_{To} + \gamma\left(\sqrt{|-2\Phi_F| + V_{SB}} - \sqrt{|-2\Phi_F|}\right) \qquad (4.1)$$

Hence gate voltage for M2 and M4 can be given as:

$$V_{G4,2} = V_{T4,2} + 2V_{ON} \qquad (4.2)$$

Gate voltage of M1 and M3 can be given as:

$$V_{G1,3} = V_{To} + V_{ON} \qquad (4.3)$$

Now it is easy to calculate value of R:

$$R = \frac{V_{G4} - V_{G1}}{I_{Ref}} \qquad (4.4)$$

Figure 4.2 shows the input output characteristics of self biased high swing cascode current mirror (SBHSCCM).

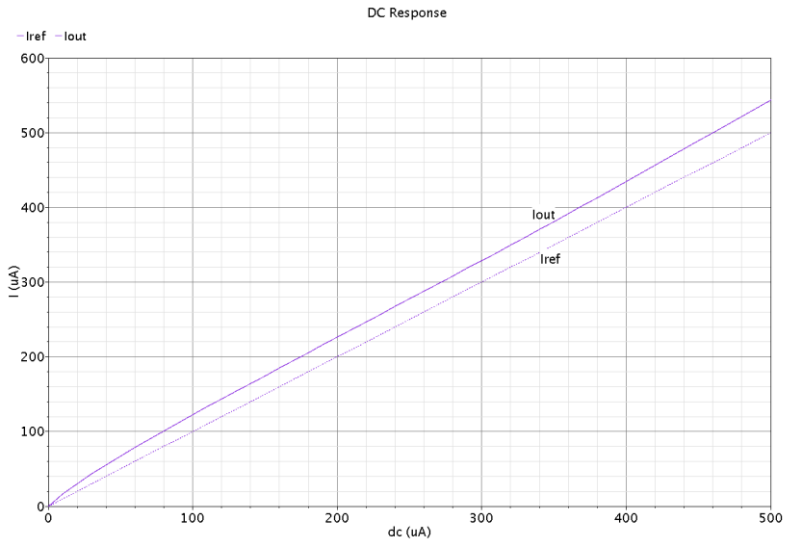

Fig. 4.2 Input Output Response of SBHSCCM.

4.2 Proposed Charge Pump

Figure 4.3 shows the proposed topology for charge pump. This is also a charge pump with switch at source. Transistors M1 to M6 accompanied with T1, T2 and T_{DN} form the DOWN circuit of charge pump, while transistors M7-M10 with T3 and T_{UP} form the complementary UP part of the circuit. This circuit does not include slow path nodes which need complex circuit to speed up. The current mirror used in this topology is designed such that all transistors are guaranteed to be in saturation. As in previous case, switches are implemented using transmission gates (TG) driven by complementary clock signals. So, it

almost removes the clock feed through effect. The output none of CP is not floating, when switches are off.

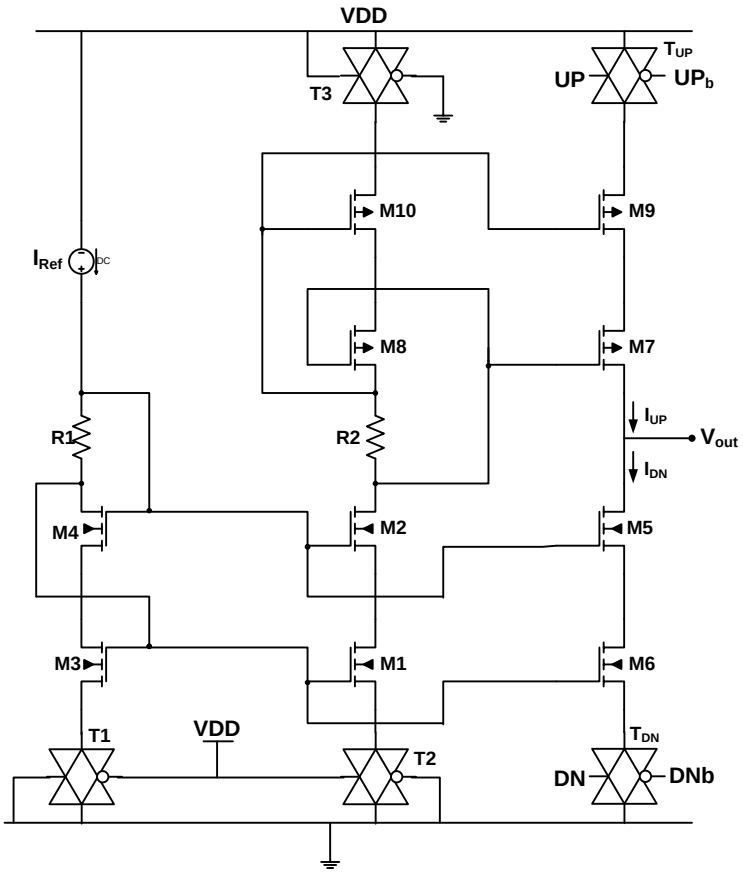

Fig. 4.3 Proposed SBHSCCM Charge Pump

Both charging and discharging currents are derived from same reference current source. Hence current mismatch is avoided. TGs T1, T2 and T3 are inserted to shun the mismatch caused due to insertion of T_{UP} and T_{DN}. The remnant current glitches which occur at the sources of output transistors (M5 and M7) while switching T_{UP} or T_{DN} would not be conveyed to the output node because of insertion of M6 and M9 as well as M5 and M7 are still of when glitches occur. Transistors M5 and M7 would be turned on softly, since rise and fall time of current pulses are controlled by the RC time constants at their sources. Hence this CP is therefore high speed CP avoiding switch errors. This statement will be clearer when simulation result will be discussed next section.

4.2.1 Design and simulation

The charge pump is design according to the procedure given in section 4.1. The reference current used is only 20µA. The W/L values of M1 to M4 are equal and also sizes of T1 and T2 are equal. But W/L values of M5- M6 and T_{DN} are 5 times smaller than M1 and T1 respectively. Similarly, sizes of M8 and M10 are equal but 5 times higher than M7 and M9. T3 is 3 times larger than T_{UP}. All this sizing has been done so as to have maximization of effective output voltage, to remove current glitches and to reduce the turn on time of PFD. Value of bias current is chosen such that charge pump helps to give minimum optimum pull in time for PLL. Figure 4.4 shows the transient response of proposed architecture while figure 4.5 shows the time verses frequency response.

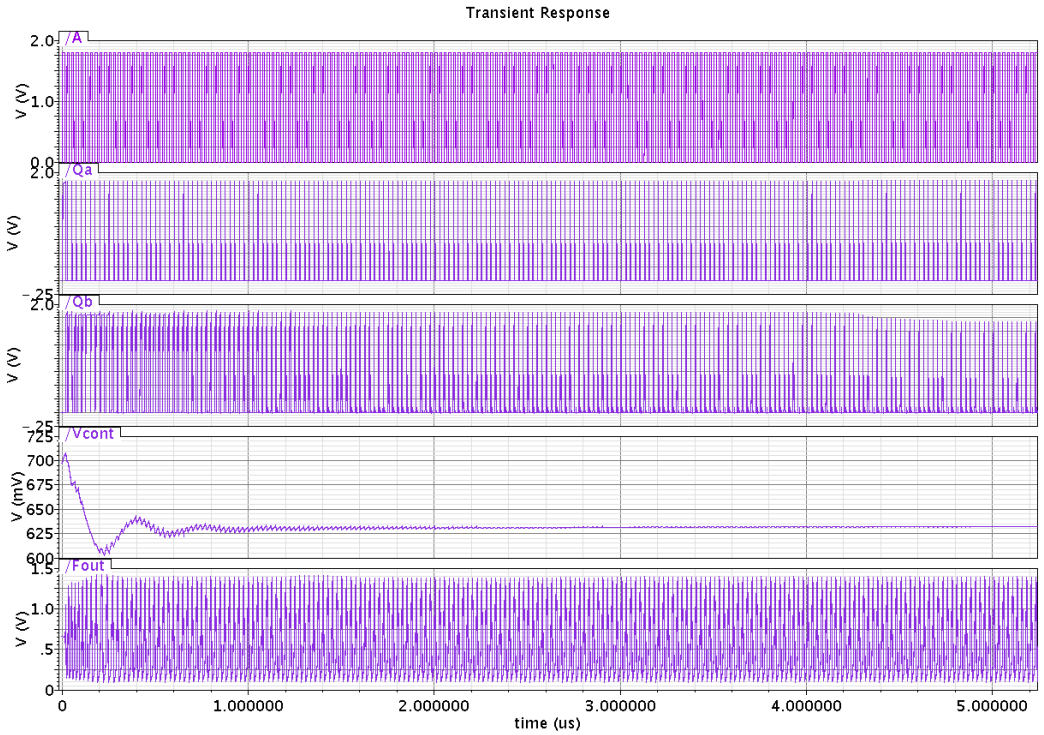

Fig. 4.4 Transient Response of Proposed CP-PLL

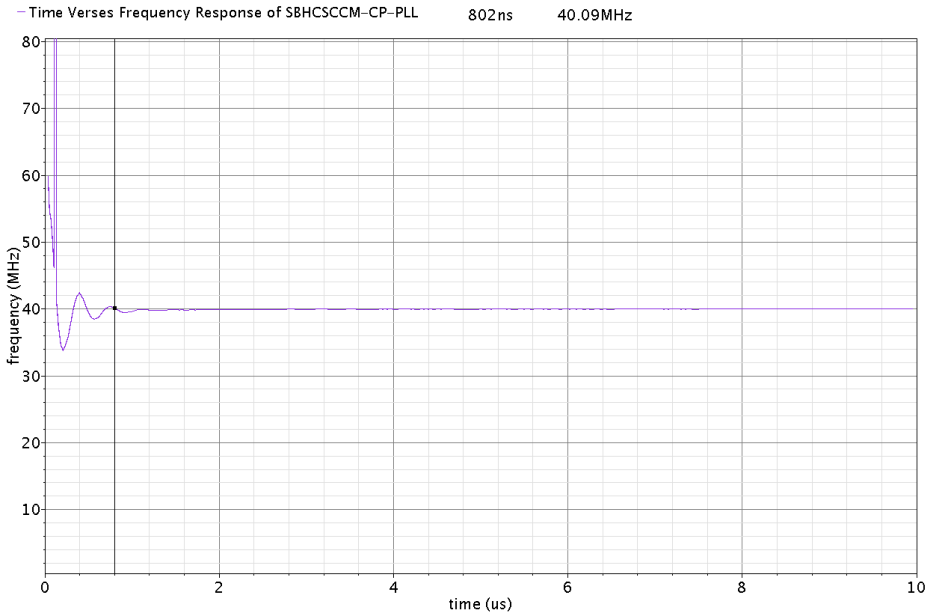

Fig. 4.5 Time Verses Frequency Response of Proposed CP-PLL

4.2.2 Discussions

1. No ripples in the control voltage, hence we can say that this topology is free from clock freed through effect and charge sharing.
2. Loop roughly locks in 850ns. Hence this topology is fastest among the topologies studied here. As said earlier, this is consequence of avoiding the switching errors.
3. Power consumption is found to be 0.6041mW, lower than source CP-PLL and TG CP-PLL.
4. Current mismatch is found to be only 2μA. The reference spur level is -64.2113dBc, lowest among all the charge pump PLLs considered here.

As said previously, choosing of proper bias current is very necessary to achieve optimum pull in time as well as to maximize effective output voltage range. If bias current is too low, obviously CP output voltage is low. Hence PLL require higher time to lock to the reference input frequency. On other hand, if bias current is too high, output voltage is also high, hence before settling to reference input, VCO frequency oscillates about reference for longer time.

This again results increase in pull in time of PLL. Table 4(a) shows the observation about bias current and pull in time of PLL.

Table 4(a) Bias Current Verses Pull In Time

I_{ref} (μA)	Pull in time of PLL (μs) (Approx.)
1.0	No Locking
1.1	No Locking
1.2	No Locking
1.3	3.0
1.4	2.8
1.5	2.66
1.6	2.53
1.7	2.4
1.8	2.0
1.9	1.89
2.0	1.66
2.5	1.57
3.0	1.57
3.5	1.2
4.0	1.14
5.0	1.0
10.0	0.97
20.0	0.802
50.0	1.13
75.0	1.34
100.0	1.73
200.0	2.9

Table 4(b) shows the summary of all architectures studied in this work.

Table 4(b) Comparison of CP architectures.

Type of CP-PLL	**Acquisition Time (Approx)**	**Power Consumption**	**Reference Spur (dBc)**	**Remark**
Basic CP-PLL	-	0.1751mW	-32.6155	Failed to acquire lock under the present design constraints , Highest reference spur
Source CP-PLL I_{REF}=500µA	4µs	1.9896mW	-61.288	Slow, requires high current, high power consumption
TG CP-PLL I_{REF}= 20µA	1.2µs	1.298mW	-48.64	Fast, not area efficient, high power consumption
Proposed SBHSCCM CP-PLL I_{REF}= 20µA	0.85µs	0.6041mW	-64.2113	Faster than TGCP, area efficient, low current requirement, low power consumption. Lowest Reference spur.

Chapter 5

Conclusions

Conclusion

1 The present work studies the important charge pump architectures and their performance.

2 A new charge pump based on High Swing Cascode Current Mirror is proposed. The proposed architecture is designed in Virtuoso Analog Design Environment in Cadence.

3 The proposed topology offers the lower power consumption compared to TG based charge pump PLL as well source charge pump PLL and has least acquisition time.

4 The PLL designed using proposed charge pump exhibits lowest reference spur of 64.211dBc. The proposed charge pump offers superior performance in many aspects as compared to other charge pump architectures.

Publications

1. Swanand Solanke, D. P. Acharya, “Design of Efficient Charge Pump in Phase Locked Loop for Wireless Communication”, *National Conference on Emerging Trends in Engineering Technology and Applications*, 2009, NCETETA09.
2. Swanand Solanke, D. P. Acharya, “Design and Synthesis of Novel Charge Pump for PLL”:- Under Preparation.

References

[1] www.uoguelph.ca/~atoon/gadgets/pll/pll.html

[2] www.altera.com

[3] http://en.wikipedia.org/wiki/Phase_locked_loop.html

[4] Behzad Razavi, "*Design of Analog CMOS Integrated Circuits",* Tata-McGraw Hill 2002, Ch. 15, pp. 532-578

[5] www.partminer.com/glossaryhtml.phase_locked_loop.html

[6] www.odyseus.nildram.co.uk/Systems_And_Devices_Files/Phasenoise.pdf

[7] www.national.com/nationaledge/feb01/286.html

[8] Dan H. Wolaver, "*Phase Locked Loop Circuit Design",* Prentice Hall, Ch. 4, pp47-80

[9] Floyd M Gardner, "Charge Pump Phase Lock Loops", *IEEE Transactions on Communication,* vol. COM-28, No. 1, pp. 1849-1858, Nov.1999.

[10] R Jakob Baker, Harry W Li, David E Boyce, "*CMOS Circuit Design Layout and Simulation",* Prentice Hall if India, 2003, Ch. 19, pp. 383-386.

[11] Wogeun Ree, "Design of High Performance CMOS Charge Pumps in Phase Locked Loop", *IEEE International Symposium on Circuits and Systems ISCAS`99,* vol. 2, June 1999.

[12] Jianzheng Zhou, zhigan Wang, "High Performance CMOS Charge Pump for phase Locked Loops", *International Conference on Microwave and Millimeter Wave Technology (ICMMT),* Vol.2, pp. 839-842, 2008.

[13] Behzad Razavi, "*Design of Analog CMOS Integrated Circuits",* Tata-McGraw Hill 2002, Ch. 5, pp. 135-165

[14] Philip E Allen, Douglus R Holburg, "*CMOS Analog Circuit Design*" 2nd Edition, Oxford University Press, 2000, pp. 131-133.